

DEPARTMENT OF THE NAVY NAVAL UNDERSEA WARFARE CENTER DIVISION NEWPORT OFFICE OF COUNSEL

PHONE: (401) 832-3653 FAX: (401) 832-4432 DSN: 432-3653



Attorney Docket No. 79479 Date: 15 August 2007

The below identified patent application is available for licensing. Requests for information should be addressed to:

PATENT COUNSEL NAVAL UNDERSEA WARFARE CENTER 1176 HOWELL ST. CODE 00OC, BLDG. 11 NEWPORT, RI 02841

Serial Number

11/183,313

Filing Date

11 July 2005

Inventor

C. Ray Dutton

If you have any questions please contact James M. Kasischke, Supervisory Patent Counsel, at 401-832-4230.

DISTRIBUTION STATEMENT Approved for Public Release Distribution is unlimited

20070822114

1	Attorney Docket No. 19419
2	
3	FIELD PROGRAMMABLE GATE ARRAY BASED GLOBAL COMMUNICATION
4	CHANNEL FOR DIGITAL SIGNAL PROCESSOR CHIPS
5	
6	STATEMENT OF GOVERNMENT INTEREST
7	The invention described herein may be manufactured and used
8	by or for the Government of the United States of America for
9	governmental purposes without the payment of any royalties
10	thereon or therefor.
11	
12	BACKGROUND OF THE PRESENT INVENTION
13	(1) Field of the Invention
14	The present invention relates to a method for networking,
15	and a network of, digital signal processors via at least one
16	field programmable gate array.
17	(2) Description of the Prior Art
18	With reference to FIG. 1, there is illustrated a typical
19	network of digital signal processors (DSP) known in the art
20	whereby a host DSP 11 is configured and programmed to globally
21	broadcast data to a multitude of non-host DSPs 15. Each non-host
22	DSP 15 is linked to the host DSP 11 by a connection between at
23	least one communication port 17 located on the host DSP 11 and at
24	least one communication port 17 on each non-host DSP 15.
25	Typically, such lines of communication are bidirectional.
26	Connecting a host DSP 11 to a multitude of non-host DSPs 15 in
27	the manner illustrated often times requires a complex and costly

- 1 patchwork of cables and connectors. Quite often, the data to be
- 2 transmitted from the host DSP 11 to each of the plurality of
- 3 non-host DSPs 15 is identical. In order to receive the data
- 4 broadcast from the host DSP 11, each non-host DSP 15 must be
- 5 physically connected via its communication port or ports 17 to a
- 6 communication port or ports 17 on the host DSP 11. This
- 7 requirement reduces the number of non-host DSPs 15 which may
- 8 receive the data from the host DSP 11 to a number no greater than
- 9 the number of communication port 17 located on the host DSP 11.
- 10 In addition to this restrictive requirement, the software which
- 11 is executed by the host DSP 11 in order to broadcast data to each
- 12 of the non-host DSPs 15 must be executed for each non-host DSP 15
- 13 connected to host DSP 11. This requirement mandates the
- 14 repetitive execution of software which is identical for each
- 15 non-host DSP 15 receiving the data communicated by host DSP 11.
- 16 What is therefore needed is a method of networking a host
- 17 DSP 11 with a plurality of non-host DSPs 15 which is neither
- 18 limited by the number of communication ports 17 located on the
- 19 host DSP 11, nor requiring the identical, repetitive execution of
- 20 software running on the host DSP 11.

21

22

SUMMARY OF THE INVENTION

- Accordingly, it is an object of the present invention to
- 24 provide a method for networking, and a network of, digital signal
- 25 processors (DSP) via at least one field programmable gate array
- 26 so as to enable the simultaneous broadcast of data from a DSP to
- 27 a plurality of DSPs.

1 In accordance with the present invention, an apparatus 2 comprising a host digital signal processor (DSP), at least one 3 field programmable gate array (FPGA) in communication with the 4 host DSP for receiving a digital signal from the host DSP, and at 5 least one non-host DSP in communication with the at least one 6 FPGA for receiving the digital signal. 7 In further accordance with the present invention, a method 8 for connecting digital signal processors comprises the steps of 9 providing a host digital signal processor (DSP), providing at 10 least one field programmable gate array (FPGA) in communication 11 with the host DSP for receiving a digital signal from the host 12 DSP, and providing at least one non-host DSP in communication 13 with the at least one FPGA for receiving the digital signal. 14 15 BRIEF DESCRIPTION OF THE DRAWINGS 16 FIG. 1 is a diagram of a network of digital signal 17 processors (DSPs) known in the art; FIG. 2 is a diagram of a network of a host DSP in 18 communication with a plurality of non-host DSPs via a field 19 20 programmable gate array (FPGA) according to the present 21 invention; and 22 FIG. 3 is a diagram of an embodiment of the present 23 invention incorporating a plurality of slave/host DSPs. 24 DESCRIPTION OF THE PREFERRED EMBODIMENTS 25 26 It is therefore an aspect of the present invention to

3

provide a method for configuring a host digital signal processor

27

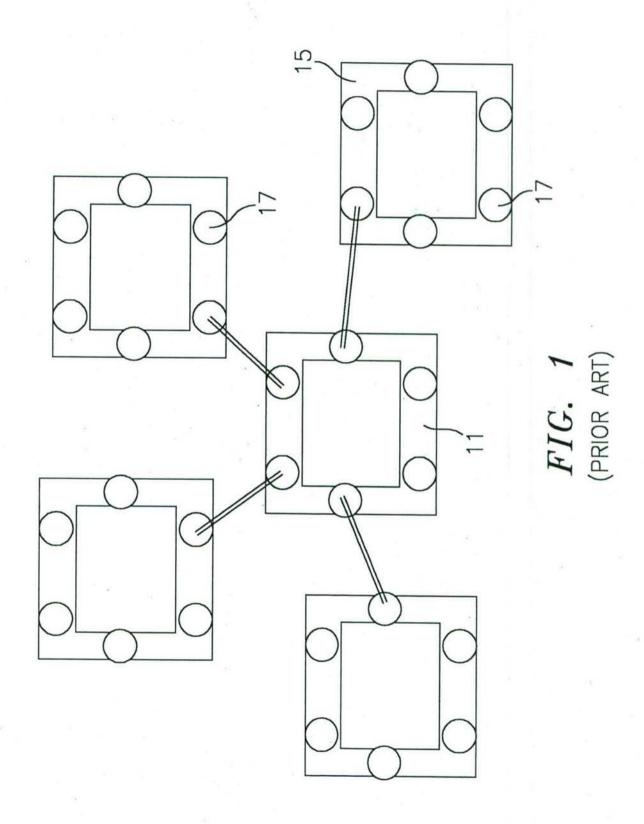
- 1 (DSP) 11 in communication with a plurality of non-host DSPs 15
- 2 wherein the number of non-host DSPs 15 receiving data broadcast
- 3 from the host DSP 11 may be greater than the number of
- 4 communication ports 17 located upon host DSP 11. Furthermore, the
- 5 method of the present invention does not require each non-host
- 6 DSP 15 to be physically connected to host DSP 11. This is
- 7 achieved by interposing a field programmable gate array (FPGA)
- 8 between the host DSP 11 and the non-host DSPs 15. The FPGA 13
- 9 serves to receive the broadcast data from the host DSP 11, to
- 10 buffer the data so received, and to handle the communication and
- 11 dissemination of the buffered broadcast data to a plurality of
- 12 non-host DSPs 15. In a preferred embodiment, host DSP 11 is
- 13 located within a host computer 33, preferably an IBM PC
- 14 compatible computer.
- With reference to FIG. 2, there is illustrated in detail a
- 16 preferred embodiment of the present invention. Host DSP 11 is in
- 17 communication with FPGA 13 via connection 19 which connects a
- 18 communication port 17 located on host DSP 11 to a communication
- 19 port 17 located on FPGA 13. Connection 19 therefore provides
- 20 bidirectional communication between host DSP 11 and FPGA 13. FPGA
- 21 13 has a plurality of additional communication ports 17 which are
- 22 utilized to communicate with a multitude of additional non-host
- 23 DSPs 15. FPGA 13 communicates with each non-host DSP 15 via a
- 24 connection 19 which connects a single communication port 17
- 25 located on FPGA 13 to a single communication port 17 located on a
- 26 non-host DSP 15. In this manner, bidirectional communication is
- 27 enabled between each non-host DSP 15 and the FPGA 13.

- In operation, host DSP 11 communicates a single stream of
- 2 data to FPGA 13 via a connection 19. It is a property of FPGAs
- 3 that they may be dynamically programmed to execute software
- 4 instructions. FPGA 13 is therefore programmed to buffer the
- 5 stream of data received by the host DSP 11 and to transmit the
- 6 received and buffered data out via the plurality of communication
- 7 ports 17 in communication with non-host DSPs 15. In addition to
- 8 transmitting the buffered data, the FPGA 13 is preferably
- 9 programmed to perform any and all initialization and data
- 10 synchronization activities required to facilitate the
- 11 communication of buffered data between the FPGA 13 and each and
- 12 every non-host DSP 15. Such communication may be either
- 13 synchronous or asynchronous. FPGA 13 is preferably constructed so
- 14 as to comprise an internal memory capable of storing, retrieving,
- 15 and returning upon request, digital data.
- In an alternative embodiment of the present invention, FPGA
- 17 13 may be in communication with an external storage device 21
- 18 wherein the data broadcast by host DSP 11 to FPGA 13 may be
- 19 buffered and stored in external storage device 21, and retrieved
- 20 by FPGA 13 as required for broadcast to the non-host DSPs 15.
- 21 External storage device 21 may be any device known in the art
- 22 capable of storing and retrieving digital data. In addition to
- 23 communicating with non-host DSPs 15, FPGA 13 may similarly
- 24 communicate with a peripheral device 23 via a communication port
- 25 17 located upon FPGA 13 and connected to the peripheral device 23
- 26 by a connection 19.
- 27 With reference to FIG. 3, there is illustrated an

- 1 alternative embodiment of the present invention. As noted above
- 2 with reference to FIG. 2, non-host DSPs 15 receive data broadcast
- 3 by host DSP 11 via FPGA 13. In such a configuration, non-host
- 4 DSPs 15 are referred to as operating in a "slave" modality with
- 5 respect to the operation of the host DSP 11. However, it is
- 6 certainly possible that one or more non-host DSPs 15 may, in
- 7 turn, act as a host DSP to one or more external devices. As
- 8 illustrated in FIG. 3, slave/host DSPs 31, 31' operate in such a
- 9 manner. There need be no physical difference between the
- 10 composition of slave/host DSPs 31, 31' and non-host DSPs 15 as
- 11 previously described. Rather, the designation of slave/host DSPs
- 12 31 by a unique reference number serve merely to differentiate the
- 13 operative roll of slave/host DSPs 31 as opposed to that of
- 14 non-host DSPs 15. Slave/host DSP 31 is connected via a connection
- 15 19 to a non-host DSP 15. Likewise, slave/host DSP 31' is
- 16 connected to an FPGA 13 via a connection 19 extending between a
- 17 communication port 17 located on slave/host DSP 31 and a
- 18 communication port 17 located on FPGA 13. It is evident that, in
- 19 this manner, the status of each non-host DSP 15 receiving data
- 20 broadcast from a host DSP 11 may be altered to that of a host DSP
- 21 11 thus earning the designation slave/host DSP 31.
- It is apparent that there has been provided in accordance
- 23 with the present invention a field programmable gate array based
- 24 global communication channel for digital signal processor chips
- 25 which fully satisfies the objects, means, and advantages set
- 26 forth hereinbefore. While the present invention has been
- 27 described in the context of specific embodiments thereof, other

- 1 alternatives, modifications, and variations will become apparent
- 2 to those skilled in the art having read the foregoing
- 3 description. Accordingly, it is intended to embrace those
- 4 alternatives, modifications, and variations as fall within the
- 5 broad scope of the appended claims.

1	Attorney Docket No. 79479
2	
3	FIELD PROGRAMMABLE GATE ARRAY BASED GLOBAL COMMUNICATION
4	CHANNEL FOR DIGITAL SIGNAL PROCESSOR CHIPS
5	
6	ABSTRACT OF THE DISCLOSURE
7	An apparatus comprising a host digital signal processor
8	(DSP), at least one field programmable gate array (FPGA) in
9	communication with the host DSP for receiving a digital signal
10	from the host DSP, and at least one non-host DSP in communication
11	with the at least one FPGA for receiving the digital signal.



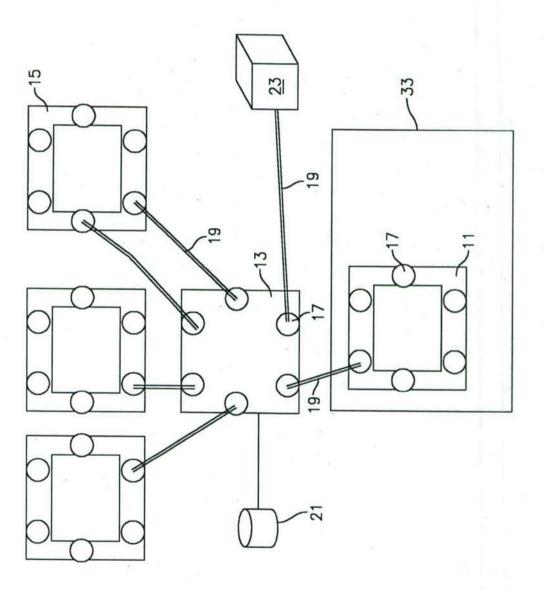


FIG. 2

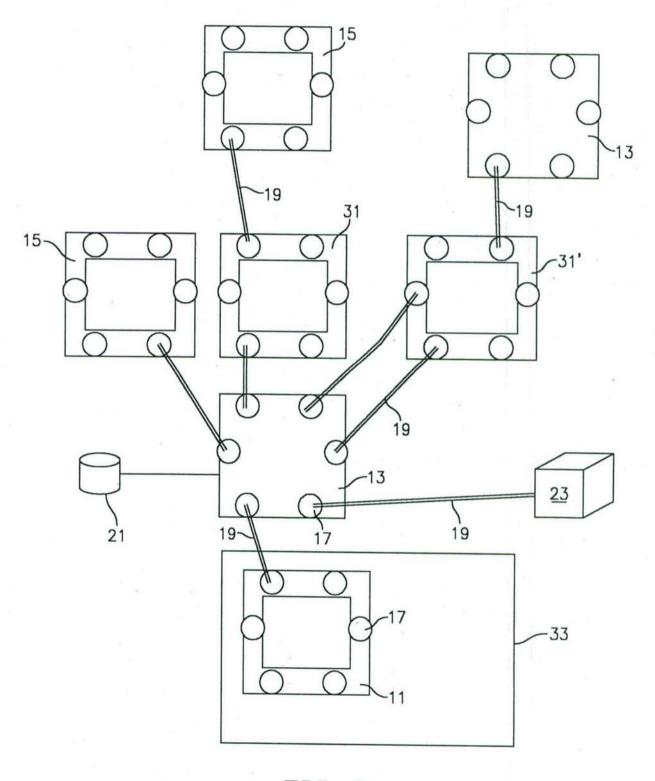


FIG. 3